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BROWN JR, NATHAN H	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/592,954	MATSUGU, MASAKAZU	
	Examiner	Art Unit	
	Nathan H. Brown, Jr.	2121	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *(3)* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *8/14/07and 3/26/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Examiner's Detailed Office Action

1. This Office is responsive to application 10/592,954, filed September 15, 2006.

2. Claims 1-24 have been examined.

Objections to the Claims

3. Claims 1, 8, 9, 18, 20, and 21 are objected to because of the following informalities: "parallelly connect(ed)" should be --connect(ed) in parallel--. Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-24 are rejected under 35 U.S.C. 102(b) as being anticipated by *Matsugu*, "Hierarchical Pulse-coupled Neural

Network Model with Temporal Coding and Emergent Feature Binding Mechanism", 2001.

Regarding claim 1. *Matsugu* teaches a parallel pulse signal processing apparatus (*see* Abstract, *Examiner interprets the "new convolutional-type, spiking neural network model with explicit timing structure of pulse trains" to be a parallel pulse signal processing apparatus*.) including a

plurality of pulse output arithmetic elements (*see* p. 802, col. 2, §2 The Convolutional Spiking Neural Network Model, *Examiner interprets "neurons of integrate-and-fire (I&F) type" to be a plurality of pulse output arithmetic elements*.),

a plurality of connection elements which parallelly connect predetermined elements of the arithmetic elements (*see* p. 802, col. 2, §2 The Convolutional Spiking Neural Network Model, Figure 1, *Examiner interprets "pulse phase modulating synapses (S) which are connected with a local bus line" to be a plurality of connection elements which connect predetermined elements of the arithmetic elements in parallel*.), and

a gate circuit which selectively passes pulse signals from the plurality of connection elements, characterized in that said arithmetic element comprises input means for inputting a

plurality of time series pulse signals (*see* p. 802, col. 2 to p. 803, col. 1, *Examiner interprets the "gating neuron (G) is also connected with a local timing neuron" to be a gate circuit which selectively passes pulse signals from the plurality of connection elements, characterized in that said arithmetic element comprises input means for inputting a plurality of time series pulse signals* .),

modulation processing means for executing predetermined modulation processing on the basis of the plurality of time series pulse signals which are input (*see* p. 803, cols. 1-2, *Examiner interprets "FD neurons detecting the same category of feature, and they extract sub-sampled data by local averaging (like in Neocognitron) or max value detection by winner-take-all mechanism from FP neurons' outputs in the receptive field" to comprise modulation processing means for executing predetermined modulation processing on the basis of the plurality of time series pulse signals which are input.*), and

pulse output means for outputting a pulse signal on the basis of a result of modulation processing (*see* p. 802, col. 2, *Examiner interprets "FD neurons" which are "spiking neurons of integrate-and-fire (I&F) type" to be a pulse output means for*

outputting a pulse signal on the basis of a result of modulation processing.), and

said gate circuit selectively passes, of the signals from said plurality of connection elements, a finite number of pulse signals (*see* p. 803, col. 1, "Each FD neuron is accompanied by an LT neuron with local receptive field similar to the FD neuron. Pulse signals from FP to FD neurons are controlled by a gating neuron G which opens the channel (local bus line) over some duration only when a control signal from an LT neuron is received.", *Examiner interprets the "duration…when a control signal from an LT neuron is received" to be of finite extent and thus the number of pulses finite in number*.) corresponding to predetermined upper output levels (*see* p. 804, col. 1, "…earlier spike arrival inside the sub-window indicates a stronger signal, and later arrival than pre-specified arrival time (e.g., t_1, t_2, in Figure 3), a weaker signal...The time window with the width of the pulse packet is divided into sub-windows, in which weighted time-domain integration of pulses is done, and the result is accumulated. Each sub-window is associated with a specific local feature to be detected.", *Examiner interprets the left boundary of each sub-window to correspond to the upper output level for its respective feature since "earlier spike arrival inside the*

sub-window indicates a stronger signal, and later arrival than pre-specified arrival time…a weaker signal”.).

Regarding claim 7. *Matsugu* teaches a parallel pulse signal processing apparatus which hierarchically executes a plurality of arithmetic processing operations (*see* Abstract and p. 802, Figure 1, *Examiner interprets the “new convolutional-type, spiking neural network model with explicit timing structure of pulse trains” to be a parallel pulse signal processing apparatus which hierarchically executes a plurality of arithmetic processing operation*.), characterized by comprising:

a plurality of arithmetic elements which receive signals from different layer levels and outputs predetermined pulse signals by a predetermined local receptor field structure (*see* p. 803, col. 2, *Examiner interprets “FD neurons detecting the same category of feature, and they extract sub-sampled data by local averaging (like in Neocognitron) or max value detection by winner-take-all mechanism from FP neurons’ outputs in the receptive field.” to be a plurality of arithmetic elements which receive signals from different layer levels and outputs predetermined pulse signals by a predetermined local receptor field structure*.); and

a gate circuit element which selectively passes the pulse signals from said plurality of arithmetic elements belonging to a predetermined receptor field in accordance with a signal level of the pulse signal (*see* p. 803, col. 1, *Examiner interprets "a gating neuron G which opens the channel (local bus line) over some duration only when a control signal from an LT neuron is received" to be a gate circuit element which selectively passes the pulse signals from said plurality of arithmetic elements belonging to a predetermined receptor field in accordance with a signal level of the pulse signal*.).

Regarding claim 8. *Matsugu* teaches a parallel pulse signal processing apparatus (*see* Abstract, *Examiner interprets the "new convolutional-type, spiking neural network model with explicit timing structure of pulse trains" to be a parallel pulse signal processing apparatus*.) including

input means for inputting data in a predetermined dimension (*see* p. 802, col. 2, §2 The Convolutional Spiking Neural Network Model, Figure 1, *Examiner interprets the "Feature pooling layer" to be an input means for inputting data in a predetermined dimension, where the predetermined dimension is the number of FP units in the "Feature pooling layer"*.),

a plurality of data processing means (*see* p. 802, col. 2, §2 The Convolutional Spiking Neural Network Model, Figure 1, *Examiner interprets the "Feature pooling layer" to be an input means for inputting data in a predetermined dimension, where the predetermined dimension is the number of FP units in the "Feature pooling layer".*),

a gate circuit which selectively passes signals from said data processing means (*see* p. 803, col. 1, *Examiner interprets "a gating neuron G which opens the channel (local bus line) over some duration only when a control signal from an LT neuron is received" to be a gate circuit which selectively passes signals from said data processing means.*), and

output means for outputting a result of pattern detection, characterized in that said data processing means includes a plurality of arithmetic elements parallelly connected by predetermined connection means (*see* p. 802, col. 2, §2 The Convolutional Spiking Neural Network Model, Figure 1, *Examiner interprets the right most "Feature detection layer" to be an output means for outputting a result of pattern detection, characterized in that said data processing means includes a plurality of arithmetic elements connected in parallel by predetermined connection means.*),

said arithmetic element included in said data processing means outputs a pulse-shaped signal train representing a detection result of a pattern of a predetermined category on the basis of an arrival time pattern of a plurality of pulses from predetermined arithmetic elements input in a predetermined time window (*see* p. 802, col. 2, "In Figure 1, each neuron in a feature detection layer, designated as FD, is coupled by pulse phase modulating synapses (S) which are connected with a local bus line." *Examiner interprets "pulse phase modulating synapses (S) which are connected with a local bus line" to be said arithmetic element included in said data processing means outputs a pulse-shaped signal train representing a detection result of a pattern of a predetermined category on the basis of an arrival time pattern of a plurality of pulses from predetermined arithmetic elements input in a predetermined time window.*), and

said output means outputs the detection result of the predetermined pattern in the data on the basis of the outputs from said arithmetic elements (*see* p. 802, col. 2, §2 The Convolutional Spiking Neural Network Model, Figure 1, *Examiner interprets the right most "Feature detection layer" to be said output means outputs the detection result of the predetermined*

pattern in the data on the basis of the outputs from said arithmetic elements.).

Regarding claim 9. *Matsugu* teaches a parallel pulse signal processing apparatus (*see* Abstract, *Examiner interprets the "new convolutional-type, spiking neural network model with explicit timing structure of pulse trains" to be a parallel pulse signal processing apparatus*.) including

input means for inputting data in a predetermined dimension (*see* p. 802, col. 2, §2 The Convolutional Spiking Neural Network Model, Figure 1, *Examiner interprets the "Feature pooling layer" to be an input means for inputting data in a predetermined dimension, where the predetermined dimension is the number of FP units in the "Feature pooling layer"*.),

a plurality of data processing means for outputting pulse signals (*see* p. 802, col. 2, Figure 1, *Examiner interprets a layer of "FD neurons" to be a plurality of data processing means (see p. 804, col. 1, §2.2 Time-window Integration of Structured Pulse Packet) for outputting pulse signals*.),

a gate circuit which selectively passes signals from said data processing means (*see* Figure. 1 and p. 802, col. 2, to p.

803, col. 1, "In Figure 1, each neuron in a feature detection layer, designated as FD, is coupled by pulse phase modulating synapses (S) which are connected with a local bus line. A gating neuron (G) is also connected with a local timing neuron, LT.", *Examiner interprets the "gating neuron (G)" and the "local timing neuron, LT" to comprise a gate circuit which selectively passes pulse signals from the data processing means (i.e., FD neurons)* .), and

output means for outputting a result of pattern detection, characterized in that said data processing means includes a plurality of arithmetic elements parallelly connected by predetermined connection means (*see* p. 802, col. 2, Figure 1, *Examiner interprets "FD neurons" which are "spiking neurons of integrate-and-fire (I&F) type" and a preceding layer of FP units to be a pulse output means for outputting a result of pattern detection (see p. 804, col. 1, §2.2 Time-window Integration of Structured Pulse Packet), characterized in that said data processing means includes a plurality of arithmetic elements connected in parallel by predetermined connection means.*),

said gate circuit selectively passes the pulse signals on the basis of signal levels of the pulse signals from said plurality of data processing means (*see* p. 803, col. 1, *Examiner*

interprets "a gating neuron G which opens the channel (local bus line) over some duration only when a control signal from an LT neuron is received" to comprise said gate circuit which selectively the pulse signals on the basis of signal levels of the pulse signals from said plurality of data processing means.),

said arithmetic elements receive a time series pulse signal (*see* p. 803, col. 1, Figure 2, *"Pulse signals from FP to FD neurons are controlled by a gating neuron G…"*),

identify time series pulse signal patterns of a plurality of classes (*see* p. 804, col. 1, §2.2 Time-window Integration of Structured Pulse Packet, *Examiner interprets the performance of "time-windowed integration of incoming pulses" such that "when the internal potential hits the threshold, the neuron fires" to identify time series pulse signal patterns of a plurality of classes since each "sub-window is associated with a specific local feature to be detected."*), and

output a pulse-shaped signal train unique to an arrival time pattern of a plurality of predetermined pulse signals input in a predetermined time window (*see* p. 804, col. 1, §2.2 Time-window Integration of Structured Pulse Packet, *Examiner interprets the performance of "time-windowed integration of incoming pulses" such that "when the internal potential hits the threshold, the*

neuron fires" to output a pulse-shaped signal train unique to an arrival time pattern of a plurality of predetermined pulse signals input in a predetermined time window since each "sub-window is associated with a specific local feature to be detected."), and

said output means outputs the detection result of the predetermined pattern in the data on the basis of the outputs from said arithmetic elements (*see* p. 804, col. 1, §2.2 Time-window Integration of Structured Pulse Packet, *Examiner interprets the performance of "time-windowed integration of incoming pulses" on the outputs from said arithmetic elements(FP neurons) by FD neurons such that "when the internal potential hits the threshold, the neuron fires" to comprise an output means that outputs the detection result of the predetermined pattern in the data on the basis of the outputs from said arithmetic elements since each "sub-window is associated with a specific local feature to be detected."*).

Regarding claim 10. *Matsugu* teaches a parallel pulse signal processing apparatus which hierarchically executes a plurality of arithmetic processing operations (*see* Abstract, *Examiner interprets the "new convolutional-type, spiking neural network*

model with explicit timing structure of pulse trains" to be a parallel pulse signal processing apparatus which hierarchically executes a plurality of arithmetic processing operations.), characterized by comprising:

input means for inputting one of an intermediate result of different layer levels and data from a predetermined memory (*see* p. 806, col. 2 to 807, col. 1, "The time-windowed integration of pulses in FD neurons with appropriate threshold could provide the system with a property of associative recall (detection) of a higher leveled feature.", *Examiner interprets the "FD neurons" to be the input means for inputting one of an intermediate result (i.e., "associative recall") of different layer levels (i.e., different FD layers) and data from a predetermined memory (i.e., "a phased-locked cluster")*.);

a plurality of data processing means, having a feature detection layer which detects a plurality of features from the data input by said input means, for outputting pulse signals (*see* p. 802, col. 2, Figure 1, *Examiner interprets a layer of "FD neurons" which are "spiking neurons of integrate-and-fire (I&F) type" and a preceding layer of FP units to be a plurality of data processing means, having a feature detection (see p. 804, col. 1, §2.2 Time-window Integration of Structured Pulse Packet) layer*

which detects a plurality of features from the data input by said input means, for outputting pulse signals.); and

a timing signal generation circuit (*see* p. 803, col. 1, "By introducing local timing inter-neuons, LT, in-between a feature pooling and a detecting layer, we embed a distributed timing (internal clock) mechanism in the system..."), said data processing means further comprising

a plurality of arithmetic elements which receive detection signals of the features of different types from a layer level of a preceding stage and output predetermined pulse signals (*see* p. 806, col. 1, Figure 5, *Examiner interprets FD neuron layers to be a plurality of arithmetic elements which receive detection signals of the features of different types from a layer level of a preceding stage via FP neuron layers and output predetermined pulse signals*.), and

a gate circuit which selectively passes outputs from said arithmetic elements involved in the plurality of predetermined features, wherein said arithmetic elements output pulse-shaped signals at one of a frequency (*see* p. 803, col. 1, "Pulse signals from FP to FD neurons are controlled by a gating neuron G which opens the channel

(local bus line) over some duration only when a control signal from an LT neuron is received. The control signal indicates the formation of phase-locked cluster (see section 4) among FP, FD, and LT neurons.", *Examiner interprets "a gating neuron G which opens the channel (local bus line) over some duration only when a control signal from an LT neuron is received" to comprise a gate circuit which selectively passes outputs from said arithmetic elements involved in the plurality of predetermined features (i.e., formation of phase-locked clusters), wherein said arithmetic elements (FP and FD neurons) output pulse-shaped signals at one of a frequency.*) and

a timing based on a plurality of input signals from said timing signal generation circuit and an arrival time pattern of a plurality of pulses in a predetermined time window (*see* p. 806, col. 1, "LT neurons, not in refractory period, spike upon a several pulses (e.g., one or two spikes) from FP neurons. A strong pulse from some LT neuron tends to ignite other LT neurons with receptive fields overlapped with that of former LT, and LT neurons with some phase lag against others become phase-locked to those with most advanced phase.", *Examiner interprets the phase-locking*

to be a timing based on a plurality of input signals from said timing signal generation circuit and an arrival time pattern of a plurality of pulses in a predetermined time window (of FD neurons).).

Regarding claim 18. *Matsugu* teaches a control method of a parallel pulse signal processing apparatus (*see* Abstract and p. 802, Figure 1, *Examiner interprets the "new convolutional-type, spiking neural network model with explicit timing structure of pulse trains" to comprise a control method of a parallel pulse signal processing apparatus*.) comprising

a plurality of pulse output arithmetic elements (*see* p. 802, col. 2, §2 The Convolutional Spiking Neural Network Model, *Examiner interprets "neurons of integrate-and-fire (I&F) type" to be a plurality of pulse output arithmetic elements*.),

a plurality of connection elements which parallelly connect predetermined arithmetic elements (*see* p. 802, col. 2, §2 The Convolutional Spiking Neural Network Model, Figure 1, *Examiner interprets "pulse phase modulating synapses (S) which are connected with a local bus line" to be a plurality of connection elements which connect predetermined elements of the arithmetic elements in parallel*.), and

a gate circuit which selectively passes pulse signals from the plurality of connection elements (*see* p. 802, col. 2, Figure. 1, *Examiner interprets the "gating neuron (G)" to be a gate circuit which selectively passes pulse signals from the plurality of connection elements (i.e., "pulse phase modulating synapses (S)")* .), characterized in that

> the arithmetic element inputs a plurality of time series pulse signals (*see* p. 802, cols. 1, *Examiner interprets "spiking neurons of integrate-and-fire (I&F) type" (e.g., FD neurons) to be arithmetic elements that input a plurality of time series pulse signals*.),
>
> executes predetermined modulation processing on the basis of the plurality of time series pulse signals which are input (*see* p. 804, cols. 1, §2.2 Time-window Integration of Structured Pulse Packet, *Examiner interprets "FD neurons which perform time-windowed integration of incoming pulses, and when the internal potential hits the threshold, the neuron fires…" to execute predetermined modulation processing on the basis of the plurality of time series pulse signals which are input*.), and

outputs a pulse signal on the basis of a result of modulation processing (*see* p. 802, col. 2, *Examiner interprets "FD neurons" to be "spiking neurons of integrate-and-fire (I&F) type" which output a pulse signal on the basis of a result of modulation processing.*), and

the gate circuit selectively passes, of the signals from the plurality of connection elements a finite number of pulse signals (*see* p. 803, col. 1, "Each FD neuron is accompanied by an LT neuron with local receptive field similar to the FD neuron. Pulse signals from FP to FD neurons are controlled by a gating neuron G which opens the channel (local bus line) over some duration only when a control signal from an LT neuron is received.", *Examiner interprets the "duration…when a control signal from an LT neuron is received" to be of finite extent and thus the number of pulses finite in number.***) corresponding to predetermined upper output levels (***see*** p. 804, col. 1, "…earlier spike arrival inside the sub-window indicates a stronger signal, and later arrival than pre-specified arrival time (e.g., t_1, t_2, in Figure 3), a weaker

signal...The time window with the width of the pulse packet is divided into sub-windows, in which weighted time-domain integration of pulses is done, and the result is accumulated. Each sub-window is associated with a specific local feature to be detected.", *Examiner interprets the left boundary of each sub-window to correspond to the upper output level for its respective feature since "earlier spike arrival inside the sub-window indicates a stronger signal, and later arrival than pre-specified arrival time…a weaker signal".*).

Regarding claim 19. *Matsugu* teaches a control method of a parallel pulse signal processing apparatus which hierarchically executes a plurality of arithmetic processing operations (*see* Abstract and p. 802, Figure 1, *Examiner interprets the "new convolutional-type, spiking neural network model with explicit timing structure of pulse trains" to comprise a control method of a parallel pulse signal processing apparatus which hierarchically executes a plurality of arithmetic processing operations.*), characterized by comprising:

causing a plurality of arithmetic elements to receive signals from different layer levels and output predetermined pulse signals by a predetermined local receptor field structure (*see* p. 803, col. 1, "By introducing local timing inter-neuons [sic], LT, in-between a feature pooling and a detecting layer, we embed a distributed timing (internal clock) mechanism in the system (detailed description in section 3). Each FD neuron is accompanied by an LT neuron with local receptive field similar to the FD neuron. Pulse signals from FP to FD neurons are controlled by a gating neuron G which opens the channel (local bus line) over some duration only when a control signal from an LT neuron is received. The control signal indicates the formation of phase-locked cluster (see section 4) among FP, FD, and LT neurons.", *Examiner interprets the "gating neuron G" to cause a plurality of arithmetic elements (FD neurons in an FD layer—see Figure 1) to receive signals from different layer levels (e.g., an FP layer level—see Figure 1) and output predetermined pulse signals(during the formation of a "phase-locked cluster") by a predetermined local receptor field structure (i.e., the local receptive field of LT neuron which is similar to the FD neuron).*); and

causing a gate circuit element to selectively pass the pulse signals from the plurality of arithmetic elements belonging to a predetermined receptor field in accordance with a signal level of the pulse signal (*see* above and p. 803, col. 1, "The FP neurons are ordinary I&F with refractoriness and generate a pulse when the internal membrane potential hits the threshold.", Examiner interprets "the internal membrane potential" hitting "the threshold" to cause a gate circuit element to selectively pass the pulse signals from the plurality of arithmetic elements belonging to a predetermined receptor field in accordance with a signal level of the pulse signal.).

Regarding claim 20. *Matsugu* teaches a control method of a parallel pulse signal processing apparatus (*see* Abstract and p. 802, Figure 1, *Examiner interprets the "new convolutional-type, spiking neural network model with explicit timing structure of pulse trains" to comprise a control method of a parallel pulse signal processing apparatus.*) comprising

input means for inputting data in a predetermined dimension (*see* p. 802, col. 2, §2 The Convolutional Spiking Neural Network Model, Figure 1, *Examiner interprets the "Feature pooling layer" to be an input means for inputting data in a predetermined*

dimension, where the predetermined dimension is the number of FP units in the "Feature pooling layer".),

a plurality of data processing means (*see* p. 802, col. 2, Figure 1, *Examiner interprets a layer of "FD neurons" to be a plurality of data processing means (see p. 804, col. 1, §2.2 Time-window Integration of Structured Pulse Packet).*),

a gate circuit which selectively passes signals from the data processing means (*see* Figure. 1 and p. 802, col. 2, to p. 803, col. 1, "In Figure 1, each neuron in a feature detection layer, designated as FD, is coupled by pulse phase modulating synapses (S) which are connected with a local bus line. A gating neuron (G) is also connected with a local timing neuron, LT.", *Examiner interprets the "gating neuron (G)" and the "local timing neuron, LT" to comprise a gate circuit which selectively passes pulse signals from the data processing means (i.e., FD neurons)* .), and

output means for outputting a result of pattern detection (*see* p. 802, col. 2, Figure 1, *Examiner interprets "FD neurons" which are "spiking neurons of integrate-and-fire (I&F) type" to be output means for outputting a result of pattern detection (see p. 804, col. 1, §2.2 Time-window*

Integration of Structured Pulse Packet.), characterized by comprising

causing each of a plurality of arithmetic elements, which are included in the data processing means and parallelly connected by predetermined connection means, to output a pulse-shaped signal train representing a detection result of a pattern of a predetermined category on the basis of an arrival time pattern of a plurality of pulses from predetermined arithmetic elements input in a predetermined time window (*see* §4 Emergent Feature Binding with Phase locked Cluster, p. 806, "Binding between lower and higher level features emerges as a natural result of interaction leading to a phase-locked cluster, as stated in the above, among FP, FD, and LT neurons. Binding between different classes (categories) of features of similar complexity (e.g., 'eye' feature and 'nose' feature in face) can also stem from the formation of phase-locked clusters among groups of FP, FD, and LT neurons (Figure 5) in charge of such categories.", *Examiner interprets the FP, FD, and LT neurons to be a plurality of arithmetic elements, which are included in the data processing means connected in parallel by predetermined connection means. Examiner interprets all*

neurons to output a pulse-shaped signal train. Examiner interprets the LT neurons to cause each of a plurality of arithmetic elements, which are included in the data processing means and connected in parallel by predetermined connection means, to output a pulse-shaped signal train representing a detection result of a pattern of a predetermined category on the basis of an arrival time pattern of a plurality of pulses from predetermined arithmetic elements input in a predetermined time window. Examiner interprets "the formation of phase-locked clusters among groups of FP, FD, and LT neurons" to represent a detection result of a pattern of a predetermined category on the basis of an arrival time pattern of a plurality of pulses from predetermined arithmetic elements input in a predetermined time window.), and

causing the output means to output the detection result of the predetermined pattern in the data on the basis of the outputs from the arithmetic elements (*see* above, *Examiner interprets the "FD neurons" to be the output means to output the detection result of the predetermined pattern in the data on the basis of the outputs from the arithmetic elements.*).

Regarding claim 21. *Matsugu* teaches a control method of a parallel pulse signal processing apparatus (*see* Abstract and p. 802, Figure 1, *Examiner interprets the "new convolutional-type, spiking neural network model with explicit timing structure of pulse trains" to comprise a control method of a parallel pulse signal processing apparatus.*) comprising

input means for inputting data in a predetermined dimension (*see* p. 802, col. 2, §2 The Convolutional Spiking Neural Network Model, Figure 1, *Examiner interprets the "Feature pooling layer" to be an input means for inputting data in a predetermined dimension, where the predetermined dimension is the number of FP units in the "Feature pooling layer".*),

a plurality of data processing means for outputting pulse signals (*see* p. 802, col. 2, Figure 1, *Examiner interprets a layer of "FD neurons" to be a plurality of data processing means (see p. 804, col. 1, §2.2 Time-window Integration of Structured Pulse Packet) for outputting pulse signals.*),

a gate circuit which selectively passes signals from the data processing means (*see* Figure. 1 and p. 802, col. 2, to p. 803, col. 1, "In Figure 1, each neuron in a feature detection layer, designated as FD, is coupled by pulse phase modulating

synapses (S) which are connected with a local bus line. A gating neuron (G) is also connected with a local timing neuron, LT.", *Examiner interprets the "gating neuron (G)" and the "local timing neuron, LT" to comprise a gate circuit which selectively passes pulse signals from the data processing means (i.e., FD neurons)* .), and

output means for outputting a result of pattern detection (*see* p. 802, col. 2, Figure 1, *Examiner interprets "FD neurons" which are "spiking neurons of integrate-and-fire (I&F) type" to be an output means for outputting a result of pattern detection (see p. 804, col. 1, §2.2 Time-window Integration of Structured Pulse Packet)*.), characterized by comprising

causing the gate circuit to selectively pass the pulse signals on the basis of signal levels of the pulse signals from the plurality of data processing means (*see* Figure. 1 and p. 802, col. 2, to p. 803, col. 1, "In Figure 1, each neuron in a feature detection layer, designated as FD, is coupled by pulse phase modulating synapses (S) which are connected with a local bus line. A gating neuron (G) is also connected with a local timing neuron, LT.", *Examiner interprets the "gating neuron (G)" and the "local timing neuron, LT" to comprise a gate circuit causing the selective*

passing of the pulse signals on the basis of signal levels of the pulse signals from the plurality of data processing means (i.e., FD neurons).),

causing a plurality of arithmetic elements, which are included in the data processing means and parallelly connected by predetermined connection means, to receive a time series pulse signal, identify time series pulse signal patterns of a plurality of classes, and output a pulse-shaped signal train unique to an arrival time pattern of a plurality of predetermined pulse signals input in a predetermined time window (*see* §4 Emergent Feature Binding with Phase locked Cluster, p. 806, "Binding between lower and higher level features emerges as a natural result of interaction leading to a phase-locked cluster, as stated in the above, among FP, FD, and LT neurons. Binding between different classes (categories) of features of similar complexity (e.g., 'eye' feature and 'nose' feature in face) can also stem from the formation of phase-locked clusters among groups of FP, FD, and LT neurons (Figure 5) in charge of such categories.", *Examiner interprets the FP, FD, and LT neurons to be a plurality of arithmetic elements, which are included in the data processing means connected in parallel*

by predetermined connection means. Examiner interprets all neurons in the model to receive a time series pulse signal. Examiner interprets the LT neurons to cause a plurality of arithmetic elements, which are included in the data processing means and connected in parallel by predetermined connection means, to receive a time series pulse signal. Examiner interprets "the formation of phase-locked clusters among groups of FP, FD, and LT neurons" to identify time series pulse signal patterns of a plurality of classes, and output a pulse-shaped signal train unique to an arrival time pattern of a plurality of predetermined pulse signals input in a predetermined time window.), and

causing the output means to output the detection result of the predetermined pattern in the data on the basis of the outputs from the arithmetic elements (*see* above, *Examiner interprets the "LT neurons" to cause the "FD neurons" to output the detection result of the predetermined pattern in the data on the basis of the outputs from the arithmetic elements.*).

Regarding claim 22. *Matsugu* teaches a control method of a parallel pulse signal processing apparatus which hierarchically

executes a plurality of arithmetic processing operations (*see* Abstract and p. 802, Figure 1, *Examiner interprets the "new convolutional-type, spiking neural network model with explicit timing structure of pulse trains" to comprise a control method of a parallel pulse signal processing apparatus which hierarchically executes a plurality of arithmetic processing operations*.), the parallel pulse signal processing apparatus comprising

input means for inputting one of an intermediate result of different layer levels and data from a predetermined memory (*see* p. 806, col. 2 to 807, col. 1, "The time-windowed integration of pulses in FD neurons with appropriate threshold could provide the system with a property of associative recall (detection) of a higher leveled feature.", *Examiner interprets the "FD neurons" to be the input means for inputting one of an intermediate result (i.e., "associative recall") of different layer levels (i.e., different FD layers) and data from a predetermined memory (i.e., "a phased-locked cluster")*.),

a plurality of data processing means (*see* p. 802, col. 2, Figure 1, *Examiner interprets a layer of "FD neurons" to be a plurality of data processing means (see p. 804, col. 1, §2.2 Time-window Integration of Structured Pulse Packet)*.),

having a feature detection layer which detects a plurality of features from the data input by the input means, for outputting pulse signals (*see* p. 802, col. 2, Figure 1, *Examiner interprets a layer of "FD neurons" to be a feature detection layer which detects a plurality of features from the data input by the input means, for outputting pulse signals.*), and

a timing signal generation circuit, characterized by comprising, under the control of the data processing means, causing a plurality of arithmetic elements to receive detection signals of the features of different types from a layer level of a preceding stage and output predetermined pulse signals (*see* p. 803, col. 1, "By introducing local timing inter-neuons, LT, in-between a feature pooling and a detecting layer, we embed a distributed timing (internal clock) mechanism in the system..."), and

causing a gate circuit element to selectively pass outputs from the arithmetic elements involved in the plurality of predetermined features (*see* Figure. 1 and p. 802, col. 2, to p. 803, col. 1, "In Figure 1, each neuron in a feature detection layer, designated as FD, is coupled by pulse phase modulating synapses (S) which are connected with

a local bus line. A gating neuron (G) is also connected with a local timing neuron, LT.", *Examiner interprets the "gating neuron (G)" and the "local timing neuron, LT" to comprise a gate circuit which selectively passes pulse signals from the data processing means (i.e., FD neurons).*), and

causing the arithmetic elements to output pulse-shaped signals at one of a frequency and a timing based on a plurality of input signals from the timing signal generation circuit (*see* §4 Emergent Feature Binding with Phase locked Cluster, p. 806, "Binding between lower and higher level features emerges as a natural result of interaction leading to a phase-locked cluster, as stated in the above, among FP, FD, and LT neurons. Binding between different classes (categories) of features of similar complexity (e.g., 'eye' feature and 'nose' feature in face) can also stem from the formation of phase-locked clusters among groups of FP, FD, and LT neurons (Figure 5) in charge of such categories.", *Examiner interprets the LT neurons to cause the arithmetic elements (the FP and FD neurons) to output pulse-shaped signals at one of a frequency and a timing (i.e., to phase-lock) based on a plurality of input signals from the timing signal generation circuit.*) and an arrival time pattern of a

plurality of pulses in a predetermined time window (*see* p. 805, col. 2, "Figure 4…Each pulse on LB indicates the one with PPM by the associated synapse. SW_L indicates a small window generated by LT neurons for the detection of phase-locking, W_{FD} is a window for integration by the FD neuron.").

Regarding claim 2. *Matsugu* teaches the apparatus according to claim 1, characterized by further comprising a timing signal generation circuit to generate a predetermined timing signal, wherein after the predetermined timing signal from said timing signal generation circuit is input, said gate circuit selectively passes, of the signals from said plurality of connection elements, the finite number of pulse signals corresponding to the predetermined upper output levels (*see* p. 803, col. 1, *Examiner interprets "a gating neuron G which opens the channel (local bus line) over some duration only when a control signal from an LT neuron is received" to comprise a timing signal generation circuit to generate a predetermined timing signal, wherein after the predetermined timing signal from said timing signal generation circuit is input, said gate circuit selectively passes, of the signals from said plurality of connection*

elements, the finite number of pulse signals corresponding to the predetermined upper output levels (of post refracted FP neurons).).

Regarding claim 3. *Matsugu* teaches the apparatus according to claim 2, characterized in that said gate circuit selectively passes, of the signals from said plurality of connection elements, the signals in ascending order of delays with respect to the timing signal from said timing signal generation circuit (*see* p. 803 col. 2 to p. 804 col. 1, *Examiner interprets the "logarithmic time scale" used to implement "spike arrival time" to map the "signal given in terms of phase (spike arrival time) from the jth class of an FP neuron at r'", $h_j(r')$, to an ascending order of delays with respect to the timing signal from said timing signal generation circuit (i.e., the gating neuron G and LT neuron—see p. 803, col. 1)*.).

Regarding claim 4. *Matsugu* teaches the apparatus according to claim 1, characterized in that said gate circuit is connected to a predetermined bus connected to said plurality of connection elements (*see* p. 802, col. 2, Figure 1, *Examiner interprets the*

"G: gating neuron" to comprise said gate circuit. Examiner interprets the "pulse phase modulating synapses (S) which are connected with a local bus line" to be connected to the "gating neuron (G)" (as shown). Examiner interprets the "local bus line" connected to the "pulse phase modulating synapses (S)" to be a predetermined bus connected to said plurality of connection elements.) and selectively passes the finite number of pulse signals (*see* p. 803, col. 1, "Each FD neuron is accompanied by an LT neuron with local receptive field similar to the FD neuron. Pulse signals from FP to FD neurons are controlled by a gating neuron G which opens the channel (local bus line) over some duration only when a control signal from an LT neuron is received.", *Examiner interprets the "duration…when a control signal from an LT neuron is received" to be of finite extent and thus the number of pulses finite in number.*) corresponding to the predetermined upper output levels from among the pulse signal propagating on the bus (*see* p. 805, col. 1, "In a short-time window (SW, in Figure 4) with a period on the order of incoming pulse width, LT neurons integrate those signals from FP neurons and detect the synchronicity among them in the integrate-and-fire dynamics; when the internal potential is over the threshold, the LT neuron feed a pulse signal to the gating neuron to open the

channel from FP neurons to the FD neuron.", *Examiner interprets "the threshold" to be predetermined.*).

Regarding claim 5. *Matsugu* teaches the apparatus according to claim 1, characterized in that said arithmetic element integrates an input pulse signal train in a predetermined time window and outputs the pulse signal at one of a phase and a frequency corresponding to the integration value (*see* p. 805, §3 Distributed Local Timing, col. 2, "Figure 4: Transition before and after the phase-locking among FP, FD, and LT neurons. LB designates a local bus line, which is shown pair-wise, for convenience, with FP. Each pulse on LB indicates the one with PPM by the associated synapse. SW_L indicates a small window generated by LT neurons for the detection of phase-locking, W_{FD} is a window for integration by the FD neuron.", *Examiner interprets a pulse signal at one of a phase and a frequency to be phase-locked.*).

Regarding claim 6. *Matsugu* teaches the apparatus according to claim 1, characterized in that said gate circuit includes a switching circuit selectively connected to, of said plurality of connection elements (*see* p. 803, col. 1 and Figure 2, *Examiner interprets Figure 2 and "Pulse signals from FP to FD neurons are*

controlled by a gating neuron G which opens the channel (local bus line) over some duration only when a control signal from an LT neuron is received" to disclose said gate circuit includes a switching circuit selectively connected to said plurality of connection elements.), a connection element whose connection strength takes a maximum value and not less than a predetermined level (*see* p. 802, col. 2, Figure 1, *Examiner interprets the "G: gating neuron" to comprise said gate circuit. Examiner interprets the "pulse phase modulating synapses (S) which are connected with a local bus line" to be connected to the "gating neuron (G)" (as shown). Examiner interprets the "local bus line" connected to the "pulse phase modulating synapses (S)" to be a predetermined bus connected to said plurality of connection elements.*).

Regarding claim 11. *Matsugu* teaches the apparatus according to claim 1, characterized in that said gate circuit includes a switching circuit selectively connected to, of said plurality of connection elements (*see* p. 803, col. 1 and Figure 2, *Examiner interprets Figure 2 and "Pulse signals from FP to FD neurons are controlled by a gating neuron G which opens the channel (local bus line) over some duration only when a control signal from an LT neuron is received" to disclose a gate circuit that includes a*

switching circuit selectively connected to said plurality of connection elements.), a connection element whose connection strength has not less than a predetermined level (*see* p. 803, col. 2, "the synaptic weight $w_{ij}(r-r')$ is provided by the weighting function M(t) defined in the subsection 2.2, which is multiplied by input spikes", *Examiner interprets the weighting function M(t) defined at equation 3 on p. 805 to have a connection strength no less than the predetermined level of 0.*).

Regarding claim 12. *Matsugu* teaches the apparatus according to claim 1, characterized in that said gate circuit selectively passes, of the signals from said connection elements (*see* p. 803, col. 1 and Figure 2, *Examiner interprets Figure 2 and "Pulse signals from FP to FD neurons are controlled by a gating neuron G which opens the channel (local bus line) over some duration only when a control signal from an LT neuron is received" to disclose that said gate circuit selectively passes, of the plurality of pulse signals.*), the signals in ascending order of delays with respect to a predetermined reference time (*see* p. 804, col. 1 and Figure 3, *"So, earlier spike arrival inside the sub-window indicates a stronger signal, and later arrival than pre-specified arrival time (e.g., t_1, t_2, in Figure 3), a weaker signal."*,

Examiner interprets that signals are passed in ascending order of delays (based on their signal strength) with respect to a predetermined reference time (based on the maxima of weight function generated by the FD neurons).).

Regarding claim 13. *Matsugu* teaches the apparatus according to claim 1, characterized in that said gate circuit selectively passes, of the plurality of pulse signals (*see* p. 803, col. 1 and Figure 2, *Examiner interprets Figure 2 and "Pulse signals from FP to FD neurons are controlled by a gating neuron G which opens the channel (local bus line) over some duration only when a control signal from an LT neuron is received" to disclose that said gate circuit selectively passes, of the plurality of pulse signals*.), the signals having a maximum output level (*see* p. 804, col. 1 and Figure 3, *"So, earlier spike arrival inside the sub-window indicates a stronger signal, and later arrival than pre-specified arrival time (e.g., t_1, t_2, in Figure 3), a weaker signal."*, *Examiner interprets that a spike at the left most boundary of sub-window t_1 to t_2 indicates a signal having a maximum output level*.).

Regarding claim 14. *Matsugu* teaches the apparatus according to claim 1, characterized in that said gate circuit selectively passes, of the signals from said connection elements (*see* p. 803, col. 1 and Figure 2, *Examiner interprets Figure 2 and "Pulse signals from FP to FD neurons are controlled by a gating neuron G which opens the channel (local bus line) over some duration only when a control signal from an LT neuron is received" to disclose that said gate circuit selectively passes the signals from said connection elements.*), a predetermined number of signals having a maximum value from an uppermost level (*see* p. 804, col. 1 and Figure 3, *Examiner interprets "earlier spike arrival inside the sub-window indicates a stronger signal, and later arrival than pre-specified arrival time (e.g., t_1, t_2, in Figure 3), a weaker signal" to disclose a predetermined (by the duration of the control signal from an LT neuron) number of signals having a maximum value from an uppermost level (determined by the sub-window width).*).

Regarding claim 15. *Matsugu* teaches the apparatus according to claim 7, characterized in that said gate circuit selectively passes pulse signals (*see* p. 803, col. 1 and Figure 2, *Examiner interprets Figure 2 and "Pulse signals from FP to FD neurons are*

controlled by a gating neuron G which opens the channel (local bus line) over some duration only when a control signal from an LT neuron is received" to disclose that said gate circuit selectively passes pulse signals.) corresponding to upper output levels for each feature (*see* p. 804, col. 1, "…earlier spike arrival inside the sub-window indicates a stronger signal, and later arrival than pre-specified arrival time (e.g., t_1, t_2, in Figure 3), a weaker signal...The time window with the width of the pulse packet is divided into sub-windows, in which weighted time-domain integration of pulses is done, and the result is accumulated. Each sub-window is associated with a specific local feature to be detected.", Examiner interprets the left boundary of each sub-window to correspond to the upper output level for its respective feature since "earlier spike arrival inside the sub-window indicates a stronger signal, and later arrival than pre-specified arrival time…a weaker signal".).

Regarding claim 16. *Matsugu* teaches a pattern recognition apparatus characterized by comprising a parallel pulse signal processing apparatus of claim 1 (*see* p. 807, col. 1, *Examiner interprets the detection* "of the structure in a pulse packet by the FD neurons involving the time-windowed integration of pulses

can be extended to multiple threshold scheme, so that a number of local feature classes can be detected, depending on the nearest threshold value not less than the resulting value of the time-windowed integration, at the same location in the input data (image)" *to disclose a pattern recognition apparatus characterized by comprising a parallel pulse signal processing apparatus of claim 1*.).

Regarding claim 17. *Matsugu* teaches an image input apparatus characterized in that pattern recognition is executed by using a parallel pulse signal processing apparatus of claim 1 (*see* p. 807, col. 1, *Examiner interprets the detection* "of the structure in a pulse packet by the FD neurons involving the time-windowed integration of pulses can be extended to multiple threshold scheme, so that a number of local feature classes can be detected, depending on the nearest threshold value not less than the resulting value of the time-windowed integration, at the same location in the input data (image)" *to disclose an image input apparatus characterized in that pattern recognition is executed by using a parallel pulse signal processing apparatus of claim 1*.), and input control of a predetermined image signal is executed on the basis of the pattern recognition result (*see* p.

806, col. 2, *Examiner interprets "…the locally distributed timing scheme that enables event-driven, stable, and precise control of pulse packet signals transmitted in the hierarchical network..." and where using "only one spike per neuron to encode a specific feature in the hierarchical, event-driven model enables extremely fast computation for the detection of some complex feature" to disclosed input control of a predetermined image signal is executed on the basis of the pattern recognition result.*).

Regarding claim 23. *Matsugu* teaches a control method of a pattern recognition apparatus characterized by comprising a parallel pulse signal processing apparatus of claim 1 (*see* p. 807, col. 1, "Detection of the structure in a pulse packet by the FD neurons involving the time-windowed integration of pulses can be extended to multiple threshold scheme, so that a number of local feature classes can be detected, depending on the nearest threshold value not less than the resulting value of the time-windowed integration, at the same location in the input data (image).", *Examiner interprets the detection "of the structure in a pulse packet by the FD neurons involving the time-windowed integration of pulses" to provide a control method of a pattern recognition apparatus characterized by comprising a parallel pulse signal*

processing apparatus (i.e., a network of "FD neurons involving the time-windowed integration of pulses").).

Regarding claim 24. *Matsugu* teaches a control method of an image input apparatus characterized by comprising executing pattern recognition by using a parallel pulse signal processing apparatus of claim 1, and executing input control of a predetermined image signal on the basis of the pattern recognition result (*see* above, *Examiner interprets the detection "of the structure in a pulse packet by the FD neurons involving the time-windowed integration of pulses" to provide a control method of an image input apparatus characterized by comprising executing pattern recognition by using a parallel pulse signal processing apparatus of claim 1, and executing input control of a predetermined image signal on the basis of the pattern recognition result.*).

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nathan H. Brown, Jr. whose telephone number is 571-272- 8632. The examiner can normally be reached on M-F 0830-1700. If attempts to reach the examiner by telephone are unsuccessful, the

examiner's supervisor, Anthony Knight can be reached on 571-272-3687. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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